AMENDMENTS TO THE CLAIMS

Claim 1 (original): A semiconductor memory device comprising

a memory cell having a variable resistive element whose electrical resistance is varied,

programming means for programming data into said memory cell using the variation of the electrical resistance of said variable resistive element,

programming state detection means for detecting variation in the electrical resistance at the time of programming operation carried out by said programming means, and

programming control means for stopping the programming operation by said programming means when the electrical resistance is varied to a predetermined reference value.

Claim 2 (original): The semiconductor memory device according to claim 1, wherein said programming state detection means can detect the variation in the electrical resistance of said memory cell by comparing the electrical resistance of said memory cell with the reference value fixed to a programming reference cell.

Claim 3 (currently amended): The semiconductor memory device according to claim [[1]] 2, wherein said programming reference cell is formed using a fixed resistance.

Claim 4 (original): The semiconductor memory device according to claim 3, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 5 (original): The semiconductor memory device according to claim 1, wherein said memory cell comprises a selection transistor and a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released.

Claim 6 (original): The semiconductor memory device according to claim 1, wherein said variable resistive element is formed with an oxide of perovskite structure having manganese between electrodes.

Claim 7 (original): The semiconductor memory device according to claim 1, further comprising

erasing means for erasing data from said memory cell using variation of said electrical resistance of said variable resistive element,

erasing state detecting means for detecting variation of said electrical resistance at the time of the erasing operation by said erasing means, and

erasing control means for stopping the erasing operation by said erasing means when the electrical resistance is varied to a predetermined second reference value.

Claim 8 (original): The semiconductor memory device according to claim 7, wherein

said programming state detection means and said erasing state detecting means are convertible to each other, and

said programming control means and said erasing control means are convertible to each other.

Claim 9 (original): The semiconductor memory device according to claim 7, wherein said erasing state detecting means can detect the variation in the electrical resistance of said memory cell by comparing the electrical resistance with the second reference value fixed to an erasing reference cell.

Claim 10 (original): The semiconductor memory device according to claim 9, wherein said erasing reference cell is formed using a fixed resistance.

Claim 11 (original): The semiconductor memory device according to claim 10, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 12 (original): A semiconductor memory device comprising

a memory cell having a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical resistance is released,

programming means for programming data into said memory cell by applying the electrical stress to said variable resistive element to vary the electrical resistance,

programming state detection means for detecting variation of said electrical resistance at the time of programming operation by said programming means, and

programming control means for stopping application of the electrical stress by said programming means when the electrical resistance is varied to a predetermined reference value.

Claim 13 (original): The semiconductor memory device according to claim 12, wherein said programming state detection means can detect the variation in the electrical resistance of said memory cell by comparing the electrical resistance with the reference value fixed to a programming reference cell.

Claim 14 (currently amended): The semiconductor memory device according to claim [[12]] 13, wherein said programming reference cell is formed using a fixed resistance.

Claim 15 (original): The semiconductor memory device according to claim 14, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 16 (original): The semiconductor memory device according to claim 12, wherein said memory cell comprises a selection transistor and a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released.

Claim 17 (original): The semiconductor memory device according to claim 12, wherein said variable resistive element is formed with an oxide of perovskite structure having manganese between electrodes.

Claim 18 (original): The semiconductor memory device according to claim 12, further comprising

erasing means for erasing data from said memory cell by applying the electrical stress to said variable resistive element to vary the electrical resistance,

erasing state detecting means for detecting variation of said electrical resistance at the time of erasing operation by said erasing means, and

erasing control means for stopping the application of electrical stress by said erasing means when the electrical resistance is varied to a predetermined second reference value.

Claim 19 (original): The semiconductor memory device according to claim 18, wherein

said programming state detection means and said erasing state detecting means are convertible to each other, and

said programming control means and said erasing control means are convertible to each other.

Claim 20 (original): The semiconductor memory device according to claim 18, wherein said erasing state detecting means can detect the variation in the electrical resistance of said memory cell by comparing the electrical resistance with the second reference value fixed to an erasing reference cell.

Claim 21 (original): The semiconductor memory device according to claim 20, wherein said erasing reference cell is formed using a fixed resistance.

Claim 22 (original): The semiconductor memory device according to claim 21, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 23 (original): A semiconductor memory device comprising

a memory cell having a variable resistive element whose electrical resistance is varied,

erasing means for erasing data from said memory cell using variation of the electrical resistance of said variable resistive element,

erasing state detecting means for detecting variation of the electrical resistance at the time of erasing operation by said erasing means, and

erasing control means for stopping the erasing operation by said erasing means when the electrical resistance is varied to a predetermined second reference value.

Claim 24 (original): The semiconductor memory device according to claim 23, wherein said erasing state detecting means can detect variation of the electrical resistance of said memory cell by comparing the electrical resistance with the second reference value fixed to the erasing reference cell.

Claim 25 (original): The semiconductor memory device according to claim 24, wherein said erasing reference cell is formed using a fixed resistance.

Claim 26 (original): The semiconductor memory device according to claim 25, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 27 (original): The semiconductor memory device according to claim 23, wherein said memory cell comprises a selection transistor and a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released.

Claim 28 (original): The semiconductor memory device according to claim 23, wherein said variable resistive element is formed with an oxide of perovskite structure having manganese between electrodes.

Claim 29 (original): A semiconductor memory device comprising

a memory cell having a variable resistive element whose electrical resistance is held even after the electrical resistance is varied by electrical stress and the electrical stress is released,

erasing means for erasing data from said memory cell by applying the electrical stress to said variable resistive element to vary the electrical resistance,

erasing state detecting means for detecting variation of the electrical resistance at the time of erasing operation by said erasing means, and

erasing control means for stopping application of the electrical stress by said erasing means when the electrical resistance is varied to a predetermined second reference value.

Claim 30 (original): The semiconductor memory device according to claim 29, wherein said erasing state detecting means can detect variation of the electrical resistance of said memory cell by comparing the electrical resistance with the second reference value fixed to an erasing reference cell.

Claim 31 (original): The semiconductor memory device according to claim 30, wherein said erasing reference cell is formed using a fixed resistance.

Claim 32 (original): The semiconductor memory device according to claim 31, wherein said fixed resistance is formed of diffused resistor or polysilicon resistor.

Claim 33 (original): The semiconductor memory device according to claim 29, wherein said memory cell comprises a selection transistor and a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released.

Claim 34 (original): The semiconductor memory device according to claim 29, wherein said variable resistive element is formed with an oxide of perovskite structure having manganese between electrodes.

Claim 35 (original): A programming method into a memory cell, wherein

said memory cell includes a variable resistive element whose electrical resistance is varied,

a programming operation for programming data into said memory cell using variation of the electrical resistance and a detecting operation for detecting variation of the electrical resistance of said memory cell at the time of the programming operation are carried out simultaneously,

the programming operation is carried out until the electrical resistance reaches a

predetermined reference value.

Claim 36 (original): A programming method into a memory cell, wherein

said memory cell includes a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released,

a programming operation for programming data into said memory cell by applying the electrical stress to said variable resistive element to vary the electrical resistance and a detecting operation for detecting variation of the electrical resistance of said memory cell at the time of programming operation are carried out simultaneously,

the application of the electrical stress is stopped when the electrical resistance is varied to a predetermined reference value.

Claim 37 (original): An erasing method from a memory cell, wherein

said memory cell includes a variable resistive element whose electrical resistance is varied,

an erasing operation for erasing data from said memory cell is carried out using the variation of the electrical resistance,

a detecting operation for detecting the electrical resistance of said memory cell at the time of the erasing operation is carried out simultaneously with said erasing operation,

said erasing operation is carried out until it is detected that the electrical resistance reaches a predetermined reference value.

Claim 38 (original): An erasing method from a memory cell, wherein

said memory cell includes a variable resistive element whose electrical resistance is varied by electrical stress and is held even after the electrical stress is released,

an erasing operation for erasing data from said memory cell is carried out by applying the electrical stress to said variable resistive element to vary the electrical resistance,

a detecting operation for detecting variation of the electrical resistance of said memory cell at the time of the erasing operation, said detecting operation and said erasing operation are carried out simultaneously,

the application of the electrical stress is stopped when the electrical resistance is varied to a predetermined second reference value.